

TRANSMITTAL OF FORMAL DRAWINGSDocket No.
FIS919970163US4
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NS
ASG*In Re Application Of: **Ronald J. Bolam, et al.**

Serial No.	Filing Date	Batch No.	Examiner	Art Unit
09/878,681	06/11/2001		Fetsum Abraham	2826

Invention: **Silicon-on-Insulator Chip Having an Isolation Barrier for Reliability**

Address to:
Assistant Commissioner for Patents
Washington, D.C. 20231

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Transmitted herewith are:

16 sheets of formal drawing(s) for this application.

OCT 09 2002
**Office of Patent Publication
Director's Office**Each sheet of drawing indicates the identifying indicia suggested in 37 CFR Section 1.84(c)
on the reverse side of the drawing.
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Dated: 9-3-02

I certify that this document and attached formal drawings
are being deposited on 9-3-02 with the U.S.
Postal Service as first class mail under 37 C.F.R. 1.8 and
addressed to the Assistant Commissioner for Patents,
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